*Indian J. Phys.* **72A** (4), 287–294 (1998)

**IJP A**
— an international journal

# Study of forward (C–V) characteristics of MIS Schottky diodes in presence of interface states and series resistance

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*Received 16 February 1998, accepted 28 April 1998*

**Abstract** : Forward (C–V) characteristics of MIS Schottky diode in presence of interface states have been studied by taking into account the effect of series resistance and using Shockley-Read-Hall statistics Exchange of charge between the metal and the interface states is included in the model It is observed that at a particular density of the interface states and a given ac signal frequency, the diode capacitance decreases in the presence of a series resistance. In addition the (C–V) plot exhibits a peak whose value depends on the interface state density and the frequency of ac signal as well as the series resistance

**Keywords** : MIS Schottky diodes, (C–V) characteristics

**PACS Nos.** : 73.30 +y, 85.30.Kk

## 1. Introduction

The origin of the excess admittance at forward-biased Schottky diodes is the subject of a controversy among research workers. Werner and coworkers [1,2] based on their experiments contend that the excess admittance observed at forward-biased Schottky diodes is due to imperfect back contacts. They ascribed the capacitance and inductance to excessive minority-carrier extraction at defective back contacts. On the other hand, Wu *et al* [3,4] attributed the excess admittance to the presence of the interface states at the boundary of the metal-semiconductor structure. Recently, Chattopadhyay and Raychaudhuri [5] investigated the frequency dependence of forward (C–V) characteristics of Schottky barrier diodes considering the series resistance effect. They found that the peak value of capacitance in (C–V) plot varies with series resistance, interface state density and the frequency of ac signal.

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In this paper, forward (C–V) characteristics of MIS Schottky diodes in presence of interface states and series resistance have been studied using Shockley-Read-Hall statistics and considering the charge exchange between the metal and the interface states.

## 2. Theoretical approach

*2.1. Determination of current density $J_{dc}$ as a function of applied voltage $V$:*

Figure 1 represents the energy band diagram of a forward biased metal/n-type semiconductor Schottky diode with a thin interfacial layer. Here $\phi_m$ is the work function of

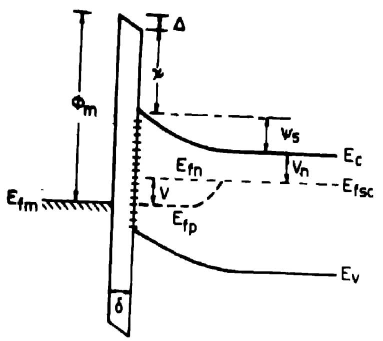


**Figure 1.** Energy band diagram of a forward biased metal/n-type semiconductor Schottky diode with a thin interfacial layer.

the metal, $\chi$ the electron affinity of the semiconductor, $\psi_s$ the semiconductor surface potential, $\delta$ the thickness of the interfacial layer, $\Delta$ the voltage drop across the interfacial layer and $V_n$ the depth of the Fermi level below the conduction band edge in the bulk semiconductor. $E_{fn}$ and $E_{fp}$ are the respective quasi-Fermi levels for electrons and holes in the semiconductor at a forward bias voltage $V$ applied to the diode.

Considering the energy band diagram, the voltage drop across the interfacial layer can be written as

$$\Delta = \phi_m - \chi - \psi_s - V_n - V + I_{dc} R_S, \tag{1}$$

where $I_{dc}$ is the current across the diode and $R_S$ the series resistance.

The voltage drop across the interfacial layer can also be obtained by using charge neutrality condition and Gauss law. Thus

$$\Delta = \quad \left(Q_{sc} + Q_{it} + Q_f\right), \tag{2}$$

where $Q_{sc}$ is the semiconductor space charge density; $Q_{it}$, the interface trapped charge density and $Q_f$, the fixed charge density in the interfacial layer.

Taking the case of the interface state continuum throughout the band gap and assuming the donor nature of the interface states, the net charge density trapped in the interface states is given by [6] :

$$Q_{it}(V_s) = q\int_{E_v}^{E_c}\left[1 - f_{it}(E_t, V_s)\right]D_{it}(E_t)\,dE_t, \tag{3}$$

where $D_{it}(E_t)$ is the interface state density at the energy level $E_t$; $V_s$, the voltage drop across the semiconductor space charge region at a forward bias voltage $V$ applied to the diode and $f_{it}(E_t, V_s)$, the occupation function of the interface states.

The occupation function of the interface state is obtained using the Shockley-Read-Hall statistics and considering the charge exchanges between metal and interface states [7–9]. Thus

$$f_{it}(E_t, V_s) = \frac{n_s + \gamma p_1(E_t)}{n_s + n_1(E_t) + \gamma\left[p_s + p_1(E_t)\right]} \tag{4}$$

where $n_s$ and $p_s$ are the quasi-thermal equilibrium densities of electrons and holes at the semiconductor surface; $n_1$ and $p_1$ are the densities of electrons and holes if their quasi-Fermi levels were coincident with trap energy level $E_t$; $\gamma$ is a parameter specifying the controllability of minority carriers on the occupancy of the interface states

In general, the description of current-voltage characteristics of most Schottky diodes is based on thermionic emission theory. Thus assuming interfacial layer-thermionic emission theory [10], the dc current density for these Schottky diodes can be written as

$$J_{dc} = A^* T^2 \theta_n \exp\left[-\frac{q}{kT}(\psi_s + V_n)\right] \quad \text{for } V \quad 3kT \tag{5}$$

where $A^*$ is the effective Richardson constant, $T$ the absolute temperature and $\theta_n$ is transmission coefficient across the interfacial layer.

The voltage dependence of surface potential $\psi_s$ can be obtained numerically from eqs. (1–3). The values of $\psi_s$ thus calculated can be used to obtain current density $J_{dc}$ as a function of applied voltage $V$.

2.2. *AC admittance of the diode* :

The ac admittance $Y$ of an MIS Schottky diode is defined as the ratio of total ac current $\delta J_{ac}$ to the ac voltage $\delta V$. Thus

$$Y = \frac{\delta J_{ac}}{\delta V} \tag{6}$$

The total ac current across the interfacial layer of an MIS Schottky diode consists of three current components :

(i) The ac current of the moving electron, given by [2]

$$\delta J_n = \frac{J_{dc}}{kT/q}\,\delta\psi_s, \tag{7}$$

(ii) The displacement current which flows within the space charge region of the semiconductor due to the change of the electric field, given by

$$\delta J_{dis} = i\omega C_{sc}\,\delta\psi_s, \tag{8}$$

where $C_{sc}$ is the semiconductor space charge capacitance.

(iii) The ac current which flows between the space charge region and the interface due to the charging and discharging of interface states, given by

$$\delta J_{it} = \left(G_{it} + i\omega C_{it}\right)\delta\psi_s, \tag{9}$$

where $G_{it}$ and $C_{it}$ represent the conductance and capacitance associated with the interface states.

With these substitutions eq. (6) becomes

$$Y = \frac{\left[\dfrac{J_{dc}}{kT/q} + G_{it} + i\omega\left(C_{sc} + C_{it}\right)\right]\delta\psi_s}{\delta V} \tag{10}$$

The expressions for $G_{it}$ and $C_{it}$ derived by Nicollian and Brews [6] for a MOS structure with interface states continuum are given by

$$G_{it} = \frac{qD_{it}(E_t)}{2\tau}\ln\left(1 + \omega^2\tau^2\right) \tag{11}$$

and

$$C_{it} = \frac{qD_{it}(E_t)}{\omega\tau}\tan^{-1}(\omega\tau), \tag{12}$$

where $\tau$ is the relaxation time of interface states and $\omega$ the angular frequency of the ac signal.

These expressions may be used to describe the interface state admittance of an MIS Schottky diode as long as the interface states are in thermal equilibrium with the semiconductor and do not communicate with the metal [11].

For a MIS diode, the variation of relaxation time $\tau$ with the applied voltage $V$ is given by [6]

$$\tau = \frac{\exp\left(q\psi_s/kT\right)}{\sigma_n \bar{v} N_d} \tag{13}$$

where $\sigma_n$ is the electron capture cross section of the interface states; $\bar{v}$ the thermal velocity of electrons and $N_d$ the donor concentration in the semiconductor.

In order to obtain the conductance $G$ and capacitance $C$ of the diode from eq. (10) one has to express $\delta\psi_s$ as a function of $\delta V$. Due to the presence of the interfacial layer and the series resistance, any voltage $V$ applied to the diode is divided across the series resistance ($V_r$), the interfacial layer ($V_i$) and the space charge region ($V_s$). Thus for small incremental change in applied voltage, we can easily write

$$\delta V = \delta V_s + \delta V_i + \delta V_r. \tag{14}$$

But $\delta V_s$ is equal to the incremental change in surface potential $\delta\psi_s$ and $\delta V_r = R_S A \delta J_{ac}$, where $A$ is the diode area. Hence

$$\delta V = \delta\psi_s + \delta V_i + R_s A \delta J_{ac}. \tag{15}$$

Taking the time derivative of incremental change in voltage drop across the interfacial layer,

$$\frac{dV_i}{dt} = \frac{1}{C_i}\left[\frac{dQ_{sc}}{dt} + \frac{dQ_{it}}{dt}\right], \quad \text{where } C_i = \epsilon_i / \delta$$

or
$$i\omega\delta V_i = \frac{1}{C_i}\left[G_{it} + i\omega(C_{sc} + C_{it})\right]\delta\psi_s. \tag{16}$$

Substituting the values of $\delta V_i$ and $\delta J_{ac}$ in eq. (15), we get

$$\frac{\delta V}{\delta\psi_s} = \alpha - i\omega\beta, \tag{17}$$

where
$$\alpha = 1 + \frac{1}{C_i}(C_{sc} + C_{it}) + R_s A\left(\frac{J_{dc}}{kT/q} + G_{it}\right) \tag{18a}$$

and
$$\beta = \frac{G_{it}}{\omega^2 C_i} - R_s A(C_{sc} + C_{it}). \tag{18b}$$

Putting this value of $\delta V / \delta\psi_s$ in eq. (10), we get

$$Y = \frac{\frac{J_{dc}}{kT/q} + G_{it} + i\omega(C_{sc} + C_{it})}{\alpha - i\omega\beta} = G + i\omega C. \tag{19}$$

Equating the real and imaginary parts on both sides of eq. (19), we get

$$G = \frac{\left(\frac{J_{dc}}{kT/q} + G_{it}\right)\alpha - (C_{sc} + C_{it})\omega^2\beta}{\alpha^2 + \omega^2\beta^2} \tag{20}$$

and
$$C = \frac{\left(\frac{J_{dc}}{kT/q} + G_{it}\right)\beta + (C_{sc} + C_{it})\alpha}{\alpha^2 + \omega^2\beta^2}. \tag{21}$$

These are the required expressions for evaluating the capacitance $C$ and conductance $G$ of the diode as a function of applied voltage $V$.

## 3. Discussion

The study has been carried out on any arbitrary metal/n-type Si Schottky diode where the metal has the work function 5.0 eV. The parameters used here are $\phi_m = 5.0$ eV, $\chi = 4.05$ eV, $N_d = 10^{16}$ cm$^{-3}$, $N_f = 5 \times 10^{11}$ cm$^{-2}$, $E_g = 1.12$ eV, $\delta = 10$ Å, $\varepsilon_s = 11.9$, $\varepsilon_i = 3.9$, $\gamma = 0.01$, $\bar{v} = 10^7$ cm/sec, $\sigma_n = 10^{-13}$ cm$^2$.

The occupancy of an interface state lying within the semiconductor bandgap depends on the charge exchange between the interface state and the three reservoirs surrounding it, namely the conduction and valence bands of the semiconductor and the conduction band of the metal. The charge exchange between the semiconductor conduction or valence bands and the interface states follows the Shockley-Read-Hall (SRH) theory while the charge exchange between the interface states and the metal conduction band occurs through direct tunneling. The occupation function $f_{it}(E_t, V_s)$ of the interface states has been calculated with the help of eq. (4). The occupation function thus obtained is used to get interface trapped charge density $Q_{it}$ from eq. (3).

Considering the interfacial layer to be of oxide layer and with $Q_{sc} = (2q\ \varepsilon_s N_d \psi_s)^{1/2}$ and $Q_f = qN_f$, $N_f$ being the density of fixed charges in the oxide layer, the values of $\psi_s$ have been calculated for different values of $V$ for a given interface state density. In obtaining the current density $J_{dc}$, we have used the values of effective transmission coefficient calculated by Card and Rhoderick [12] for oxide films of thickness from 8 Å to 26 Å.

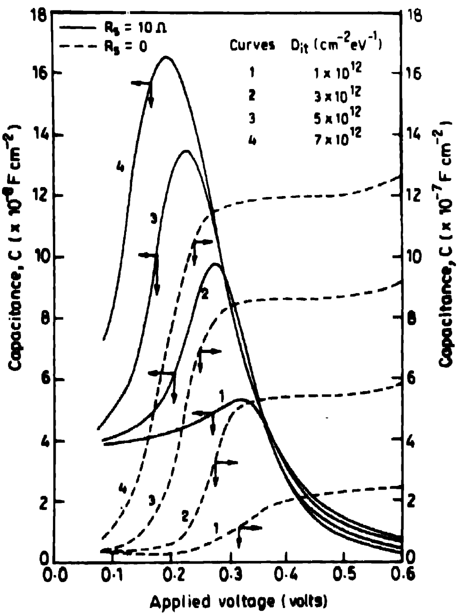


**Figure 2.** Forward (C–V) characteristics of an MIS Schottky diode at $\omega = 2\pi \times 10^4$ Hz with interface state density as parameter.

Figure 2 shows the effect of interface state density on the forward (C–V) characteristics of the diode at $\omega = 2\pi \times 10^4$ Hz. It is obvious from the figure that the diode capacitance $C$ increases with the increase of the density of interface states in both situations (*i.e.*, $R_s = 0$ and $R_s = 10\ \Omega$). This is because of the presence of the interface states at the boundary of the interfacial layer/semiconductor, which attribute the interface state admittance thus modifying the diode capacitance $C$. It may be noted that at a particular density of the interface states, the value of $C$ decreases in the presence of a series resistance. This is due to the voltage drop across the series resistance $R_s$ which in turn, increases the value of $\delta V / \delta \psi_s$ and thus decreases the diode admittance according to eq. (10). Further, in the presence of a series resistance the (C–V) plot exhibits a peak whose value increases and also shifts towards a lower voltage as the density of the interface states increases. The capacitance peak in (C–V) plot has been observed in a number of experimental studies on Schottky diodes [13–15]. However, here the results regarding the capacitance peak position with the interface state density differ from those obtained by Chattopadhyay and Raychoudhuri [5]. This discrepancy may be due to the relaxation time dispersion of the interface states.

Figure 3 represents the frequency dependence of the forward (C–V) characteristics of the diode at $D_{it} = 5 \times 10^{12}$ cm$^{-2}$ eV$^{-1}$. It is seen that in both situations (*i.e.*, $R_s = 0$ and $R_s = 10\ \Omega$), the diode capacitance $C$ increases in the lower voltage region with the decrease of the frequency of ac signal. This happens because at lower frequencies, the interface states respond the ac signal and yield the excess capacitance. However, in higher voltage region, the capacitance $C$ does not change. This is due to the large relaxation time of the interface states lying near the conduction band edge. These inferences are in consistent with the experimental results observed by Barret and Vapaille [16], and Singh [17].

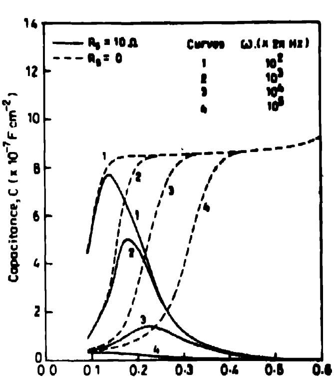


Figure 3. Frequency dependence of the forward (C–V) characteristics of the diode at $D_{it} = 5 \times 10^{12}$ cm$^{-2}$ eV$^{-1}$. Other parametric values are the same as those used in Figure 2.

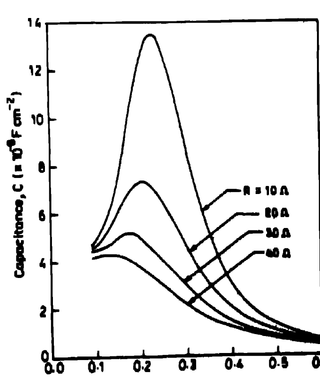


Figure 4. Effect of the series resistance on the forward (C–V) characteristics of an MIS Schottky diode at $D_{it} = 5 \times 10^{12}$ cm$^{-2}$ eV$^{-1}$ and $\omega = 2\pi \times 10^4$ Hz. Other parametric values are the same as those used in Figure 2.

Effect of series resistance on the (C–V) characteristics of the diode at $D_{it}$ = $5 \times 10^{12}$ cm$^{-2}$ eV$^{-1}$ and $\omega = 2\pi \times 10^4$ Hz is shown in Figure 4. It is observed that the capacitance plot exhibits a peak whose value strongly depends on the values of the series resistance. As the series resistance increases, the peak value of the capacitance decreases and also shifts towards a lower voltage. Similar results have been reported by Chattopadhyay and Raychoudhuri [5] and Venkatesan *et al* [18].

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